What is claimed is:

1. A process for growing a GaAs epitaixial layer on Ge/SiGe/Si substrate comprising steps of :

(1) providing a clean silicon wafer;

(2) growing a first SiGe epitaixial layer with a certain thickness, which the layer comprises at least 70 wt.% of Ge;

(3) performing in-situ high temperature annealing for the first layer;

(4) growing a second and/or an optional third layers which the Ge content of the optional third layer is more than that of the second layer, and second layer hereof is more than that of the first one. During each of two growing periods, performing in-situ high temperature annealing for those layers;

(5) growing a pure Ge film on the epitaixial layer from step (4) ;

(6) finally, growing GaAs epitaxy on said Ge film.

2. The process according to Claim 1,

wherein, in steps (1) to (5), the Ge content of epitaixial layers, from the first layer, the second and/or third layer to a pure Ge film as the topmost lay, is stepwise increasing , and their growth is carried out at a temperature of from 350 to 650℃, growth gases having pressure of from 20 to 100 m-Torr by using ultra-high vacuum chemical vapor deposition; in addition, in step (6), growing for GaAs epitaxy is carried out at a temperature of 600℃ by using metal organic chemical vapor deposition and the growth time depends on the device requirement.

3. The process according to claim 1 or 2, wherein the first SiGe epitaixial layer is $Si_{0.1}Ge_{0.9}$ which has a thickness of at least 0.1 μ m.

4. The process according to claim 3, wherein the first SiGe epitaixial layer is $Si_{0.1}Ge_{0.9}$ which has a thickness of 0.5 to 0.8 μ m.

5. The process according to claim 1 or 2, wherein the second SiGe epitaixial layer is $Si_{0.05}Ge_{0.95}$ which has a thickness of at least 0.1 μ m.

6. The process according to claim 5, wherein the second SiGe epitaixial layer is $S_{i0.05}Ge_{0.95}$ which has a thickness of 0.5 to 0.8 μ m.

7. The process according to claim 1 or 2, wherein the optional third SiGe epitaixial layer is $Si_{0.02}Ge_{0.98}$ which has a thickness of at least 0.1 μ m.

8. The process according to claim 7, wherein the optional third SiGe epitaixial layer is $Si_{0.02}Ge_{0.98}$ which has a thickness of 0.5 to 0.8 μ m.
9. The process according to claim 1, wherein the first SiGe epitaixial layer can comprise 70 to 90 wt.% of Ge.
10. The process according to claim 1, wherein the second SiGe epitaixial layer can comprise 80 to 95 wt.% of Ge.
11. The process according to claim 1, wherein growing for epitaxy layer is carried out at a temperature of 400℃.
12. The process according to claim 1 or 2, wherein in-situ high temperature annealing is performed at a temperature of 750℃ in at least 5 min.
13. The process according to claim 12, wherein the atmosphere of in-situ high temperature annealing is hydrogen with a pressure of 20 m-Torr.
14. The semiconductor structure of SiGe epitaxy, comprising a silicon substrate, a first SiGe epitaixial layer having Ge content at least 70 wt.% , a second SiGe epitaixial layer having Ge content more than that of the first layer, an optional third SiGe epitaixial layer having Ge content more than that of the second layer, a pure Ge film, and a GaAs epitaixial layer as the topmost layer, characterized in that the first SiGe epitaixial layer can accommodate large dislocations which are generated and located near in the low of part of the first layer and the interface due to the large lattice mismatch, and the second and/or the optional third layers can form strained interfaces of said layers to bend and terminate the propagated upward dislocation very effectively.
15. A semiconductor structure of SiGe epitaxy, comprising a silicon substrate, a first SiGe epitaixial layer having Ge content at least 70 wt.% , a second SiGe epitaixial layer having Ge content more than that of the first layer, an optional third SiGe epitaixial layer having Ge content more than that of the second layer, a pure Ge film, and a GaAs epitaixial layer as the topmost layer, characterized in that the thickness of epitaixial layers totally is controlled in not exceed to 3.0 μ m, and the surface of said layers is very smooth and without planarization using CMP.
16. A semiconductor structure of SiGe epitaxy, comprising a silicon substrate, a first SiGe epitaixial layer having Ge content at least 70 wt.% , a second SiGe epitaixial layer having Ge

content more than that of the first layer, an optional third SiGe epitaixial layer having Ge content more than that of the second layer, a pure Ge film, and a GaAs epitaixial layer as the topmost layer, characterized in that the threading dislocation density is controlled in not exceed to $10^6/cm^2$ in a process according claim 1.

17. The semiconductor structure according to any one of claims 14 to 16 is suitable as high-speed devices and optical devices.

18. The semiconductor structure according to any one of claims 14 to 16 is further suitable as a wafer of Group III-IV material and an integrating wafer which is used to integrate Group III-IV material and Group IV material.